International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Scalable DC Model of High Voltage SOI-LDMOS

Lekshmi.T, Beena S., Nadheera K. M.
Department of Electronics and Communication Engineering,
Government Engineering College, Barton Hill, Thiruvananthapuram

Abstract — **This paper presents a scalable dc model for high voltage silicon on insulator lateral double diffused MOS (SOI-LDMOS) transistor scaled for different geometries as well as temperatures, assuming uniform doping for the channel. The device is analyzed and curves for velocity and voltages are plotted, for each of the device regions. Based on this analysis, the model is developed. Here MM20 model is used for the channel and drift region under the thin gate oxide. New model developed for the drift region under the field oxide, which exhibits quasi-saturation, is scaled for different lengths of the channel region, the drift region under the thin gate oxide and drift region under thick gate oxide, by taking into consideration the results of analysis. Also taken into account is the drift length modulation, at high gate and drain voltages. Temperature dependent modeling of the device is also done. The model developed exhibits high level of accuracy with the device simulated using MEDICI, over wide range of temperatures and different lengths of each of the regions.**

Keywords — **DC Modeling, LDMOS, Quasi-Saturation, Scalable Model, SOI Technology.**

I. INTRODUCTION

HVICs and Smart PICs merge the power devices with the low voltage circuitry on a single chip and thus provide a suitable alternative to discrete circuits in a wide variety of automobile and consumer applications [1]. Lateral diffused MOSFETs implemented in bulk silicon or SOI form an integral part of these circuits. One of the features needed for the realization of such ICs is the isolation between the power device and the low voltage circuitry. This is remarkably provided by SOI technology and hence SOI LDMOS are now preferred especially in Smart Power ICs [2]. In addition, fabricating LDMOS on a SOI platform also offers the advantage of high packing density and less leakage current. Thus an accurate model for SOI-LDMOS describing its device characteristics accurately over a wide range of biases, temperatures and device dimensions, is needed to predict the behavior of these circuits at all operating conditions.

Fig.1. shows the cross section of a high voltage SOI-LDMOS. The LDMOS is an asymmetric device with a drift region located between the channel and the heavily doped drain contact. The channel region is self aligned to the gate and is created by the diffusion of p-body under the gate. The source is then formed by diffusion. Since the channel and the source are formed by successive diffusion steps, these devices are called as lateral double diffused transistors. The drift region of the HV-LDMOS is very long as compared to a low voltage LDMOS so as to withstand externally applied high voltages. The channel region (Reg-I) for the device under discussion is considered uniformly doped for simplicity of modeling. The point 'Di ' indicates the abrupt transition from Reg-I to the n-drift region. The n-drift region comprises of the region under the thin gate oxide (Reg-II) and the region under the field oxide (Reg-III). The transition from Reg-II to Reg-III is represented by 'D' '. The entire drift region is lightly doped to withstand high operating voltages. Thus the depletion region extends more into Reg-II as compared to Reg-I. The length of the drift region varies with increase in the voltage blocking capability of the device. There is no significant extension of the gate electrode on Reg-III. Also the field oxide is also very thick. The entire transistor is isolated from the bulk by a buried oxide making it a SOI device. The important dimensions of the HV LDMOS devices are the length of the Reg-I (L_{ch}), the length of the Reg-II (L_{dr}) and the length of the Reg-III (L_{LOCOS}) as is indicated in Fig.1.

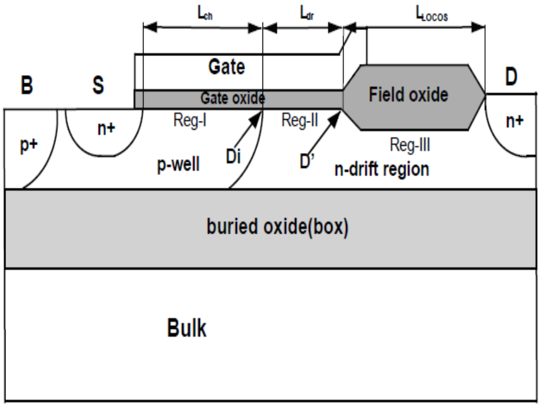

Fig.1. Cross-sectional view of a HV SOI LDMOS device

The paper is structured as follows. Section II deals with the phenomenon of quasi-saturation. Section III discusses its modeling. Section IV comprises the results of the model implementation. Conclusions are presented in Section V.

II. THEORY OF QUASI-SATURATION

To provide accurate model for the HV-LDMOS its electrical behavior needs to be analyzed and understood. This requires the separation of the HVLDMOS into the specific regions i.e. Reg-I, Reg-II, Reg-III. This separation is not physical but only formal to understand the device behavior in a much better fashion.

The LDMOS has in common with the conventional MOSFETs, the Reg-I and hence the LDMOS can be considered as a low voltage MOSFET in series with the drift region. The advantage of this approach is that we can use the already available surface potential models to describe various phenomena occurring in Reg-I and focus on the effects occurring in the drift region like accumulation/depletion under Reg-II and quasi-saturation occurring in Reg-III. To explain the device operation, the operating range of gate voltage is divided into two regions: Low to moderate V_{GS} and High V_{GS}.

Doping profile of the device under study is as shown in Fig.2.

For low values of applied V_{GS} greater than the threshold voltage of Reg-I, electrons are attracted to the surface to form an inversion layer in Reg-I. An accumulation layer is formed under the gate in Reg-II in response to this V_{GS}. On the application of V_{DS}, electrons flow takes place from source, though Reg-I, Reg-II, Reg-III to drain. When V_{DS} is increased, it leads to increased electric field in Reg-I, finally leading to velocity saturation in Reg-I. Velocity saturation also occurs in the Reg-II at even higher V_{DS}, after velocity saturation taking place in the Reg-I. So the saturation of current is controlled by the channel region.

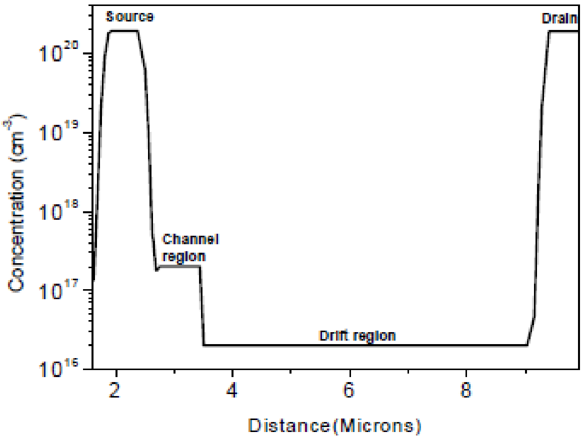

Fig.2. Doping profile showing the source and drain doping, the channel doping and the drift region doping

When V_{GS} is high, inversion layer electron concentration in Reg-I and accumulation layer electron concentration in Reg-II also starts to rise in an exponential fashion. The increased conductivities in this region cause the voltage in both the regions to decrease. The result is an increase in voltage drop across Reg-III. The velocity in Reg-III starts to rise and finally at high V_{GS}, it approaches the saturation velocity as can be observed from Fig. 3. Thus, it is Reg-III which is responsible for the reduction in current at high V_{GS} values. This is termed as quasi-saturation effect in high voltage MOSFETs as is shown in Fig. 4. Hence the current saturation in this device at high V_{GS} is due to velocity saturation in the Reg-III. When V_{DS} is increased further, the depletion width at the drain end of the Reg-III increases. This leads to a shorter drift length in Reg-III (the effect which may be termed as drift length modulation) which leads to an increase in the drain to source current with increasing drain voltages.

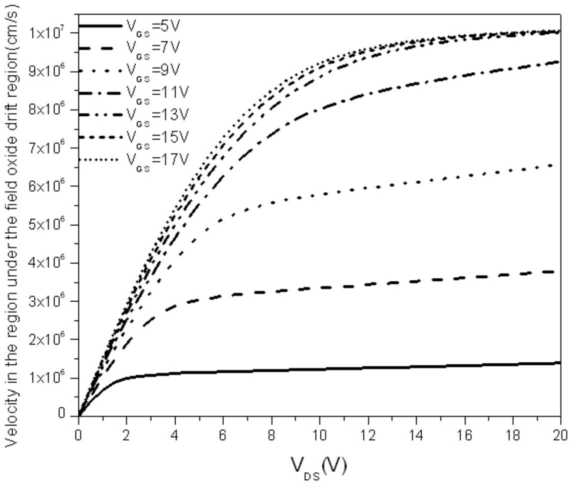

Fig.3. Velocity in the drift region under the gate oxide obtained from Medici simulations**.**

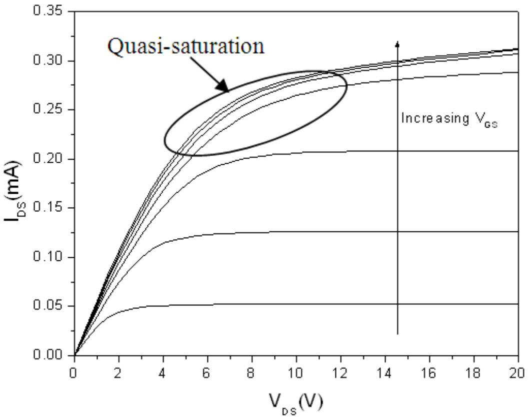

Fig.4. I_{DS}-V_{DS} plot obtained from MEDICI simulations for High Voltage LDMOS device

As the external temperature is increased from very low to high values, the mobility of the electrons starts to fall because of the lattice scattering prevalent at high temperatures. This has the tendency to decrease the value of current. The temperature rise in the device also leads to a drop in the flat band voltage and fermi potentials of Reg-I and Reg-II. This will decrease the threshold for current conduction resulting in a rise in the current. At low values of V_{GS}, the reduction in flat band voltage will be the dominant mechanism. Thus, at low values of V_{GS}, the current rises with increase in temperature.

At moderate values of applied V_{GS}, with increase in temperature it is seen that the current starts to drop because the mobility reduction overrides decrease in flat band voltage. Also the carrier saturation velocity decreases as temperature is raised due to the scattering effects resulting in a drop in current in the quasi-saturation region.

In Existing compact models, models developed for low voltage LDMOS has been extended to high voltage LDMOS by adding a constant resistance to model the region under the thick field oxide [3, 4]. For high V_{GS}, as V_{DS} is increased, the voltage drop in the region under the field oxide (Reg-III) goes on increasing, resulting in the electric field in that region to go above the critical electric field leading to velocity saturation. Thus the current saturates due to velocity saturation in Reg-III. Hence Reg-III cannot be modeled as a constant resistance. A new compact model which takes into account this aspect is developed [5]. In this paper this model has been extended for different lengths of the drift region under the gate oxide and field oxide. Temperature scaling as well as drift length modulation is also included in the model equation.

III. MODELING METHODOLOGY

A. Model Without Temperature Parameters

1) Equation For The Channel Current: Channel current is formulated using surface potential approach [4] so that a continuous description of drain current and its derivative .is obtained.

$$I_{ch} = (1+\lambda_{ch}V_{DiS})\frac{W\mu_{effch}C_{ox}}{L_{ch}}\frac{(V_{inv0}-0.5\xi V_{DiSeff})V_{DiSeff}}{1+\theta_{3ch}V_{DiSeff}} \quad (1)$$

Here *W* is the width of the device, C_{ox} is the gate oxide capacitance and $V_{inv0}=Q_{inv0}/C_{ox}$ where Q_{inv0} is the inversion layer charge per unit area at the source side. ξ is the deviation of the inversion layer charge with the change in surface potential. The parameter θ_{3ch} takes into consideration the velocity saturation in Reg-I. μ_{effch} is the effective mobility of the electrons in the Reg-I with reduction due to the vertical electric field also modeled. V_{DiSeff} is the effective potential drop across the Reg-I. V_{DiSeff} is the minimum of V_{DiS} and the channel saturation voltage V_{satch}. λ_{ch} considers channel length modulation.

2) Equation For The Current In The Drift Region Under The Gate Oxide: The major two effects occurring in Reg-II are: velocity saturation due to the lateral electric field and accumulation due to vertical electric field. Here drift component of current is only taken into account. The current equation is [4]

$$I_{dr} = W\mu_{effdr}C_{ox}\frac{\left[V_{ndr}|_{V_c=V_{Di}} - 0.5\xi_{dr}V_{D'Dieff}\right]V_{D'Dieff}}{L_{dr}(1+\theta_{3dr}V_{D'Di})} \quad (2)$$

μ_{effdr} is the effective mobility of electrons in Reg-II with mobility reduction due to vertical electric field accounted for. The term θ_{3dr} considers velocity saturation in this region. The voltage V_{ndr} is given by $V_{ndr}=Q_{ndr}/C_{ox}$. Q_{ndr} is the charge density per unit area in Reg-II. $V_{D'Dieff}$ is the effective potential drop across Reg-II, which is the minimum of $V_{D'Di}$ and the drift saturation voltage V_{satdr}. Here ξ_{dr} is taken as 1.

3) Equation For The Current In The Drift Region Under The Field Oxide: In Reg-III, model [5] is scaled for different geometries and temperatures. The current through Reg-III takes into account the velocity saturation and drift length modulation in the region, and is given by

$$I_{dr1} = (1+\lambda_{dr1}V_{DD'})\frac{qN_{dr1}\mu_{dr1}V_{DD'}Wt_{si}}{L_{LOCOS}\left(1+\theta_{1dr1}\left(\frac{V_{DD'}}{L_{LOCOS}E_C}\right)^{\theta_{dr1}}\right)^{\frac{1}{\theta_{dr1}}}} \quad (3)$$

Here t_{si} is the thickness of Reg-III. $V_{DD'}$ is the voltage drop across the Reg-III. N_{dr1} is the doping of the Reg-III and μ_{dr1} is the mobility of electrons in this region. θ_{1dr1} and θ_{dr1} represent parameters for the velocity saturation in the Reg-III. λ_{dr1} is drift length modulation parameter.

E_C is the critical electric field at which velocity saturation occurs and is given by

$$E_C = \frac{v_{sat}}{\mu_{dr1}}. \quad (4)$$

where v_{sat} is the saturation velocity of electrons.

The implemented dc model equivalent circuit is as shown in Fig.5.

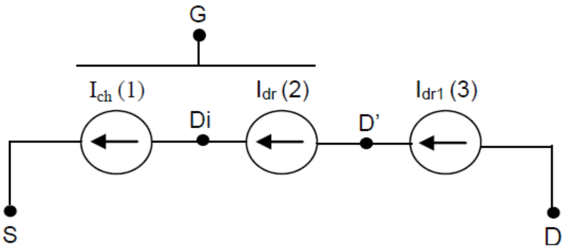

Fig.5. DC model equivalent circuit showing the internal nodes Di and D'.

B. Temperature Dependent Modeling

For an LDMOS, there are several parameters that are temperature dependent. But for avoiding complexity in modeling, the temperature dependencies of some of the parameters need only be considered to completely determine the effect of the temperature on the LDMOS behavior.

The carrier mobility decreases with temperature due to increased scattering.

$$\mu_{eff,T} = \mu_{eff,T_0}\left(\frac{T}{T_0}\right)^{-k_m} \quad (5)$$

Here $\mu_{eff,T}$ is the effective mobility at temperature T and $\mu_{eff,T0}$ is the effective mobility at ambient temperature T_0. Every mobility dependent model parameter is described as power functions of temperature.

Other parameters which are dependent on temperature are the surface potential required for strong inversion ϕ_0 and the flat band voltage V_{FB} and carrier saturation velocity v_{sat}. ϕ_0 depends on the Fermi-potential ϕ_B, which in turn is a function of temperature as well as band-gap Eg. V_{FB} is temperature dependent through ϕ_{MS}. A linear variation for both with temperature is quite justifiable.

Carrier saturation velocity is also a function of temperature. An empirical model is used to describe the temperature dependence of v_{sat}.

$$v_{sat} = \frac{2.4e7}{1+0.8415\frac{T}{600}} \quad (6)$$

Critical field is defined in terms of the mobility and the carrier saturation velocity and is modeled accordingly.

IV. RESULTS AND DISCUSSIONS

Device simulation is carried out with the structure in Fig.1 and doping concentration in Fig.2 using commercially available device simulator MEDICI [6].

Implemented Verilog-A [7] model is simulated using Spectre [8] from Cadence. The model is compared with MEDICI results as reference.

A. With Change in Length of Channel Region

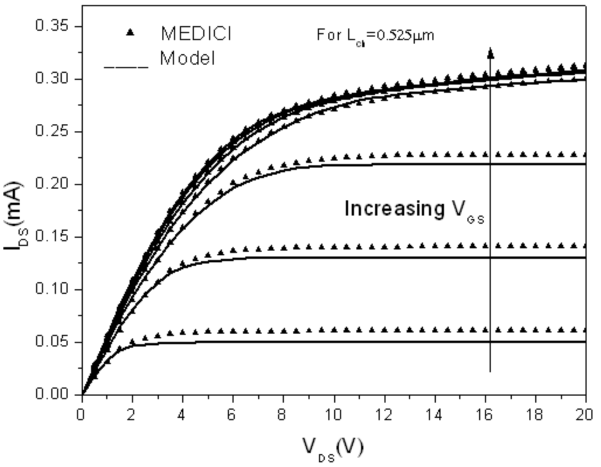

Fig.6. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=0.525μm, L_{dr}=2.25 μm, L_{LOCOS}=3.65 μm].

As the channel length (L_{ch}) decreases, the current in the Reg-I will increase resulting in an increase in the drain current as can be perceived from Fig. 6 and Fig. 7. But the upper limit of the current is determined by the drift region under the field oxide based on the quasi-saturation of this region and hence the upper limit of the current does not vary much based on the change in length of the Reg-I. As can be observed from Fig. 6 and Fig. 7, the model accurately reproduces the MEDICI simulation results for the device.

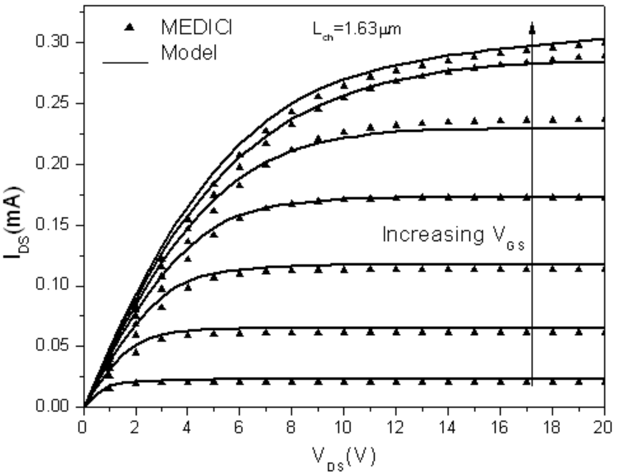

Fig.7. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=1.63μm, L_{dr}=2.25 μm, L_{LOCOS}=3.65 μm].

B. With Change in Length of Drift Region Under Gate Oxide

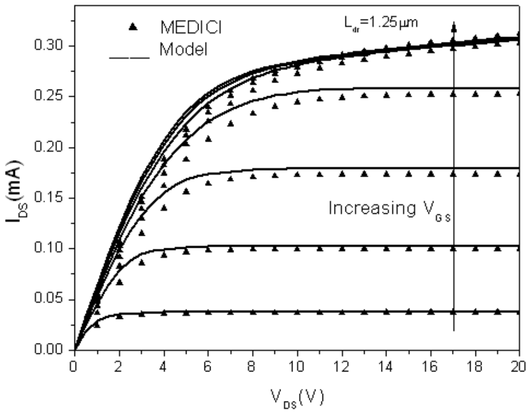

Fig.8. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=0.825μm, L_{dr}=1.25 μm, L_{LOCOS}=3.65 μm].

When the length of Reg-II (L_{dr}) is increased, it will result in the current in Reg-II to decrease as seen in Fig.8 and Fig. 9.Thus, changing L_{dr} will lead to a reduction of drain current in the linear region. It also leads to slight decrease in the current at the transition from linear region to saturation region and quasi-saturation region. These are the regions of the characteristics where Reg-II behavior alters the LDMOS characteristics. The quasi-saturation behavior of the device is not affected by variation of length of Reg-II. Also saturation of current at low V_{GS} values is not altered by change in L_{dr}.

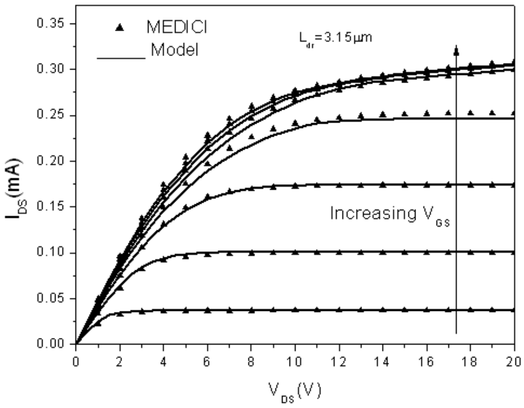

Fig.9. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=-0.825μm, L_{dr}=3.15 μm, L_{LOCOS}=3.65 μm].

Fig. 8 and Fig. 9 shows the model plots compared with the MEDICI plots for various lengths of drift region under gate oxide and it can be seen that the model predicts the LDMOS behavior accurately.

C. With Change in Length of Drift Region Under Field Oxide

It can be seen from Fig. 10 and Fig. 11 that the decrease in length of Reg-III (L_{LOCOS}) causes the quasi-saturation region of the device characteristics to be altered. The current in quasi-saturation region increases with reduction in the length of Reg-III. This is because as the length of Reg-III is reduced, velocity saturation in Reg-III occurs at lower values of V_{DS} resulting in quasi-saturation. This is followed by drift length modulation resulting in slight increase in the current with increase in V_{DS}. As L_{LOCOS} is raised, the slope of the current in the quasi-saturation region decreases. Thus, the length of Reg-III limits the maximum currents that can be achieved in an LDMOS transistor. It is also observed that saturation of current at lower V_{GS} values is not affected by the change in L_{LOCOS}, as this is predominantly due to Reg-I. Fig. 10 and Fig.11 compare the model results for different lengths of the drift region under field oxide against MEDICI simulations. It can be observed that the model is able to predict accurately the behavior of the device in the region under field oxide.

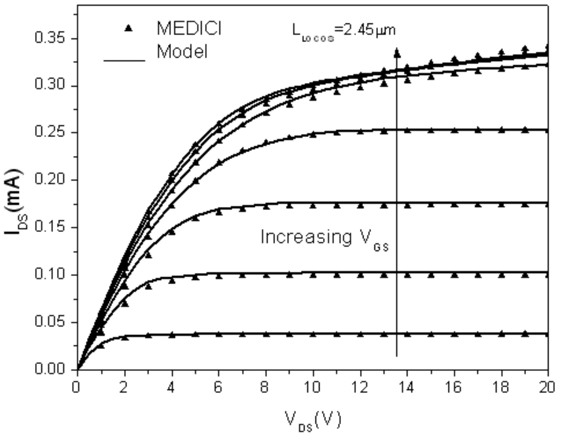

Fig.10. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=-0.825μm, L_{dr}=2.25 μm, L_{LOCOS}=2.45μm].

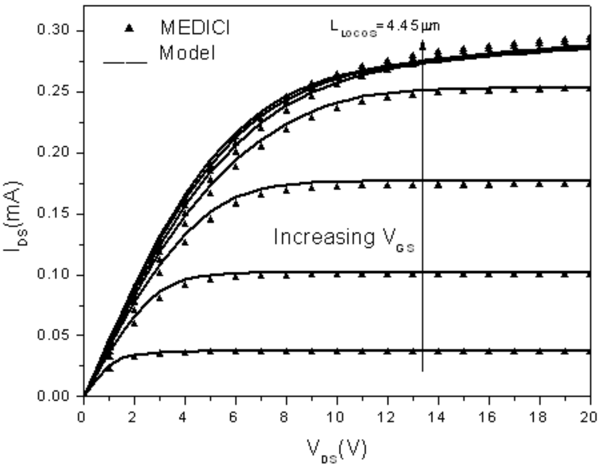

Fig.11. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=-0.825μm, L_{dr}=2.25 μm, L_{LOCOS}=4.45μm].

D. Scaling With Variation in Temperature

Effect of variation of temperatures from 10°C to 127°C on the drain characteristics of the LDMOS is shown in Fig.12 and Fig.13. With increase in temperature, effect of the flat band voltage is seen as a increase in current at low V_{GS} while at moderate and high V_{GS}, the current reduces due to decrease in mobility. Fig.12 and Fig.13 plots the drain currents obtained from the model against device simulation for different temperatures. It is found that the model reproduces the behavior of the device at different temperatures with good accuracy. Hence the effect of temperature on the drain characteristics of LDMOS is effectively reproduced here by considering the temperature models for the mobility, flat band voltage, fermi potential and carrier saturation velocity as is explained.

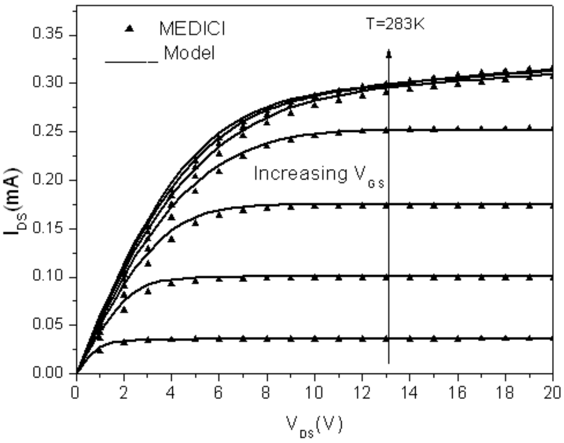

Fig.12. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=-0.825μm, L_{dr}=1.25 μm, L_{LOCOS}=2.45μm and T=283K].

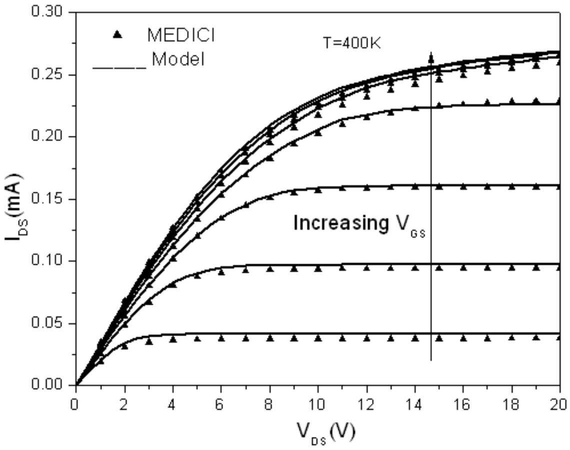

Fig.13. I_{DS}-V_{DS} plot obtained from MEDICI simulations against the new model for V_{GS}=5V, 7V, 9V, 11V, 13V, 15V, 17V and V_{SB}=0V [L_{ch}=-0.825μm, L_{dr}=1.25 μm, L_{LOCOS}=2.45μm and T=400K].

V. CONCLUSION

A scalable model based on the principle of quasi-saturation in the drift region under the thick field oxide is developed. The model is scalable for all the three regions viz. channel, drift region under the gate oxide and drift region under field oxide. The above model is also scalable for all operating temperatures. Results of the model are compared with MEDICI device simulations and found to be accurate.

REFERENCES

[1] K. Sakamoto, N. Fuchigami, K. Takagawa and S. Ohtaka, "A Three-Terminal Power MOSFET with Built-In Reverse Battery Protection for Automotive Applications", *IEEE Transaction on Electron Devices*, 1999, Vol. 46, No. 11, pp. 2228-2234.

[2] A. C. T. Aarts, M.J. Swanenberg and W.J. Kloosterman, "Modeling of High Voltage SOI-LDMOS Transistor including self-heating," *Proceedings of International Conference on Simulation of Semiconductor Devices and Processes* (SISPAD 2001).

[3] A. C. T. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surface potential-based high-voltage compact LDMOS transistor model," *IEEE Trans. Electron Devices*, vol. 52, No. 5, pp. 999–1007, Mar. 2005.

[4] A.C.T Aarts and Willy.J.Kloosterman,"Compact Modeling of High-Voltage LDMOS Devices Including Quasi-Saturation," *IEEE Transactions on Electron Devices* vol.53, No.4, April 2006.

[5] Lekshmi T, Amit Kumar Mittal, Amitava DasGupta, Anjan Chakravorty, "Compact Modelling of SOI-LDMOS including Quasi-saturation Effect", International Workshop on Electron Devices and Semiconductor Technology (IEDST 2009).

[6] Taurus Medici User's Guide, Version V-2003, Synopsis Inc, Mountain View, CA, 2003.

[7] Verilog-AMS Language Reference Manual, Version 2.2 available at www.designers-guide.org/VerilogAMS.

[8] Virtuoso Spectre Circuit Simulator User Guide, Version 7. 0.1, June 2008 available at www.d.umn.edu/~htang/Cadence_doc.

AUTHOR'S PROFILE

Lekshmi T.

received her B.Tech degree in Electronics engineering from Cochin University of Science and Technology in 2002 and M.Tech degree in Microelectronics and VLSI from I.I.T., Madras in 2009.

She started her teaching career in 2004 as Lecturer in Electronics and Communication Engineering under Cochin University of Science and Technology. In 2005, she joined as lecturer in Electronics and Communication Engineering at Government Engineering College, Barton Hill, Thiruvananthapuram, India. She is currently working as Assistant Professor in Electronics and Communication Engineering at Government Engineering College, Barton Hill, Thiruvananthapuram. She has published a conference paper titled "Compact Modelling of SOI-LDMOS including Quasi-saturation Effect" that appeared in Proceedings of International Workshop on Electron Devices and Semiconductor Technology (IEDST 2009) at I.I.T Bombay. Her areas of research interest includes semiconductor device modeling and digital VLSI system design. Lekshmi T is a member of IEEE society.

Beena S.

did her B.Tech degree in Electronics and Communication from University of Kerala in 2003. She is currently pursuing her M.Tech in Microwave Engineering from College of Engineering, Thiruvananthapuram under University of Kerala.

She has worked as Lecturer in Electronics and Communication Engineering from 2008 to 2009, after which she joined as a lecturer in Electronics and Communication Engineering at Government Engineering College, Barton Hill, Thiruvananthapuram, She is currently working as Assistant Professor in Electronics and Communication Engineering at Government Engineering College, Barton Hill, Thiruvananthapuram. Her research areas include Device modeling, Image Processing and Product Design. She has presented a paper titled 'Digital image Tampering Detection based on Wavelet Transform' at National Conference on Emerging Technologies at Government Engineering College, Barton Hill, Thiruvananthapuram. Beena S is a life member of ISTE.

Nadheera K. M.

received her B.Tech in Electronics Engineering from Model Engineering College under Cochin University of Science and Technology in 1995.She did her M.Tech from College of Engineering, Trivandrum in Applied Electronics and Instrumentation in 2005.

She worked as a Lecturer in Electronics and Communication Engineering in College of Engineering, Chengannur from 1996-2001 and College of Engineering, Karunagappally from 2001-2002 both under IHRD. Later she joined as a lecturer in Electronics and Communication Engineering at Government Engineering College, Barton Hill, Thiruvananthapuram in 2002. She is currently working as Assistant Professor in Electronics and Communication Engineering at Government Engineering College, Barton Hill, Thiruvananthapuram. Her research areas include Device modeling, Image Processing and Signal Processing. She has presented a paper titled 'Determination of Hidden Messages in Still Images using Neural Networks' at National Conference on Technological Trends. Nadheera K.M is a life member of ISTE.